DESIGN WORKSHOP TECHNOLOGIES

Verification and Analysis

Major Product Features

- Comprehensive DRC for micro-electronics
- Extended capabilities for MEMS and Photonics
- User-defined DRC region
- DRC commands and ruledecks fully supported by the scripting language
- Proven accuracy and support for true all-angle and man-hattan structures
- Complete Boolean operators and derived layers that are distortion free due to superior algorithms
- Available in 2 versions: batch and fully integrated with the dw-2000™ layout platform

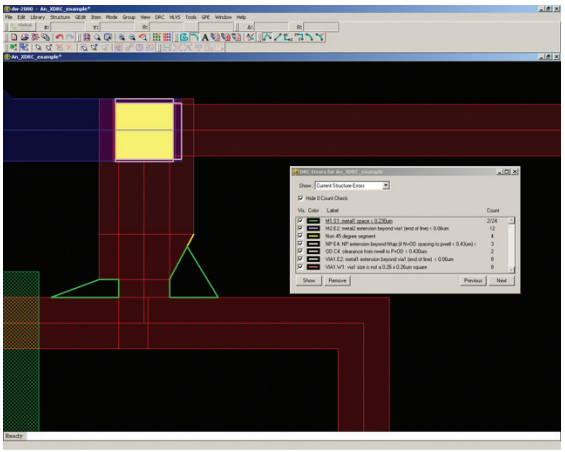
True all-angle Layout Verification Software

Layout verification and the support of subsequent analyses, such as post-layout simulation, are proven risk reduction factors. The early identification and correction of layout structures is of vast importance in order to ensure consistently high yielding wafers.

Verification has become increasingly more difficult due to the convergence of more complex device structures and smaller feature sizes. The industry's desire to augment functionality on a single substrate will continue to strain the capabilities of conventional verification software.

Design Workshop Technologies provides designers with proven design rule check (DRC), extraction, and layout versus schematic (LVS) software modules. Development by *Design Workshop Technologies* guarantees industry leading numerical precision and algorithms designed to ensure stable, accurate handling of these diverse structure types.

Micro-electronic DRC



In addition to conventional design rule checks, the powerful rule deck language – GPE – easily handles complex rule checking of antenna rules, end-of-line rules and off-grid rules. Graphic programming environment language is the common scripting language used by all *Design Workshop Technologies*' dw-2000 products. Using GPE increases the layout designer's productivity in two ways: language re-use and the ability to incorporate rule checks into user macros. Productivity is further ensured through detailed graphical error navigation and correction. In addition, designers can perform rule checks on any user-specified region.

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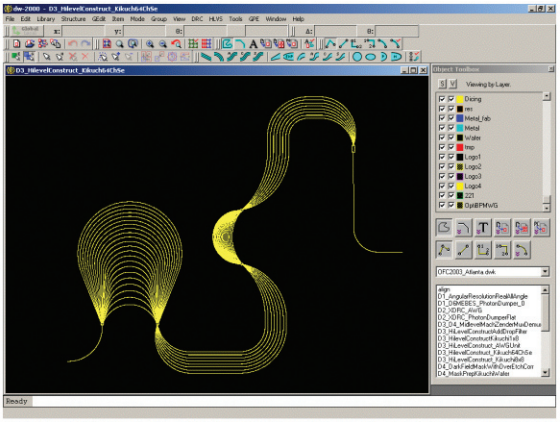
LVS/Extraction *Highlights*

- Layout versus Layout
- Layout versus Schematics
- Extract inductors and other complex user-defined devices
- Spice netlist format for device level simulation

DRC for the unconventional



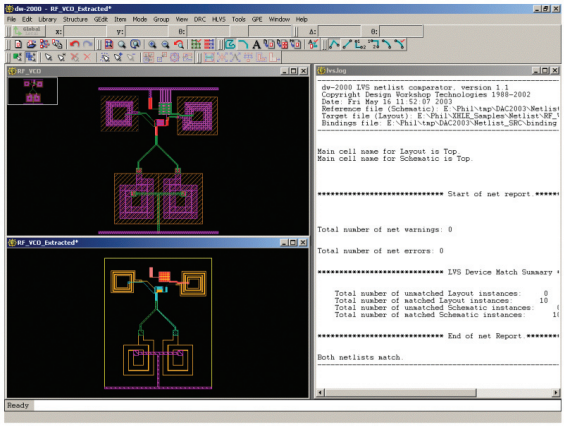
Device categories, such as planar light circuits (PLC), require additional support for Boolean operations to create derived layers and for design rule checks of complex curve linear structures. The GPE scripting and rule deck language easily sustains new checks, such as:

- Minimum bend radius rules
- Identification of misaligned waveguides
- User-defined rules …

"…I think what sets DW aside from most competitors is the extremely powerful programming language, which provides immense extendibility…"

Richard J Bojko
Seagate Technology

HLVS and Extraction



An optional dw-2000 HLVS module provides layout designers with both netlist extraction and LVS functionality. Users can compare layout against layout and layout against schematics.

This module supports the extraction of traditional devices such as transistors, resistors, capacitors, diodes, and nets, in addition to the identification of inductors. *Design Workshop Technologies*' dw-2000 software also supports the extraction of user-defined devices.

Design Workshop Technologies

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