DESIGN WORKSHOP TECHNOLOGIES

DW 2000 Physical Layout and Verification Software

HLVS

HLVS • Hierarchical Layout Extractor and Layout Versus Schematic

dw-2000 HLVS is the gateway to advanced features such as electrical layout extraction and network comparison. As is true with all dw-2000 modules, HLE and LVS are well integrated with the dw-2000 programming environment (GPE) and easily customized to address a wide variety of problems. With these modules, you can easily implement extraction rules for any technology or application.

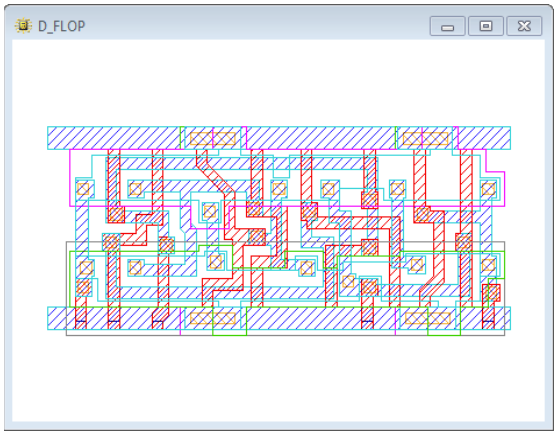
Hierarchical Layout Extraction

HLE is an electrical extractor that translates the physical geometric organization of a circuit layout into an electrical network (or netlist). Based on user defined relationship information, it proceeds to detect electrical components from the geometrical relationships of the layout. The extractor then generates a HSPICE netlist with device parameters and with or without parasitic devices.

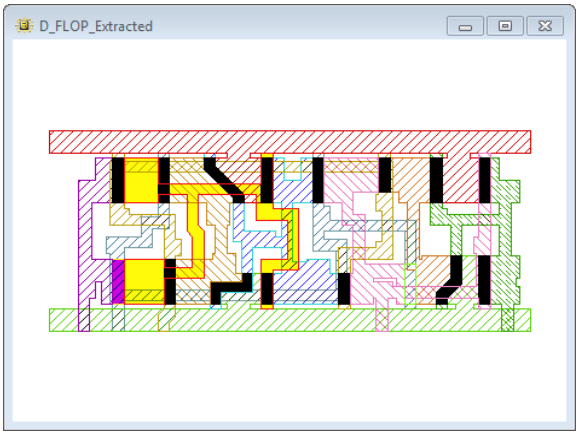
Flat or Hierarchical Extraction

HLE allows you to choose between hierarchical or flat extraction. In the case of a hierarchical extraction, you can select which nested structures to instantiate as "leaf cells" in the netlist. This powerful feature allows the layout hierarchy to be different than the reference netlist hierarchy, thereby freeing you from having to apply the same hierarchy to your layouts.

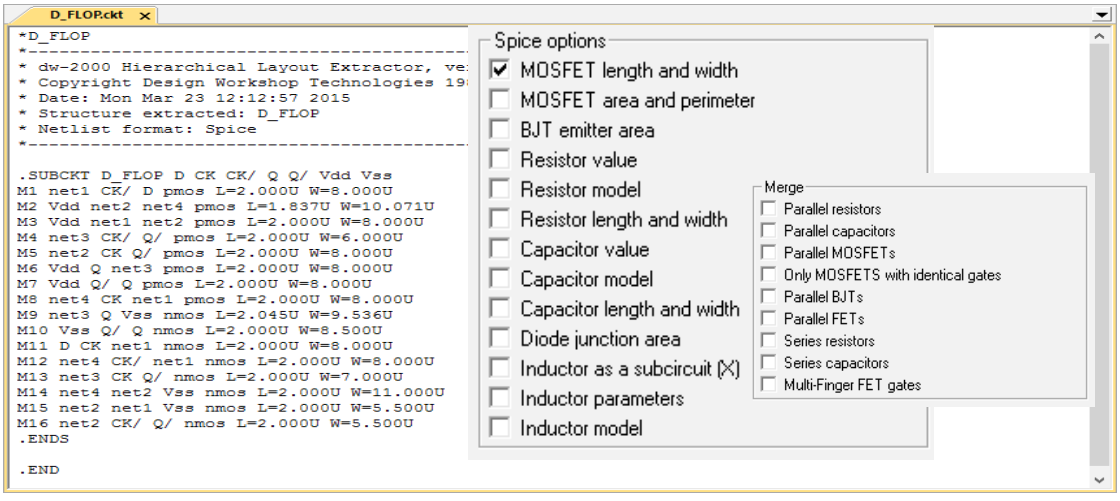
Source Design



Extracted View showing devices and networks



Netlist with device parameters



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Optimize your yield
with high quality verification software

HLE *Highlights*

- HLE commands are GPE-scriptable; hence usable in users' programs
- Generate Hierarchical or Flat netlists
- Parasitics extraction
  - Resistors
  - Overlap and Fringe Capacitors
  - User defined parasitic devices
- Electrical view representation and navigation
- Easy Net and Device navigation
- Flexible device extraction including:
  - Transistors (Bi-Polar, FET, MOS, ...)
  - Diodes
  - Resistors
  - Inductors
  - Capacitors
  - User defined devic

LVS *Highlights*

- LVS support of HSPICE, EDIF and VERILOG
- Name-binding option for matching non symmetrical cell representations
- Matching tolerance
- Pin swapping control
- Ability to merge parallel and serial devices
- Exhaustive LVS reports
- Ambiguity depth search control for Net matching

dw-2000 *Highlights*

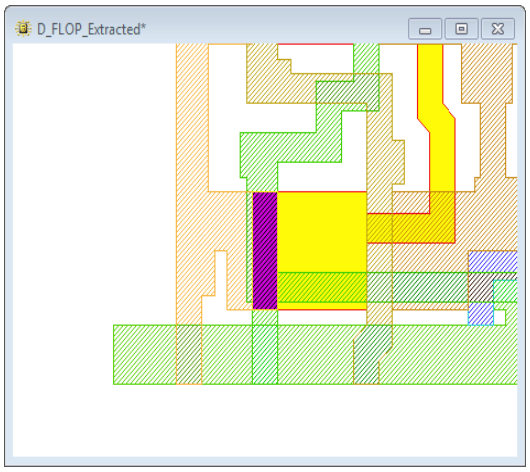
- Native 64bit editions for increased speed and performance
- Hierarchical layout
- All-angle Boolean and resize
- Fully customizable
- Programming language environment
- Automatic layout generation
- Fully-featured
- Unlimited undo/redo
- View at different aspect ratios
- Snapping using Gravity
- Conversion to/from other formats
- Parametric Cells (P-Cells)

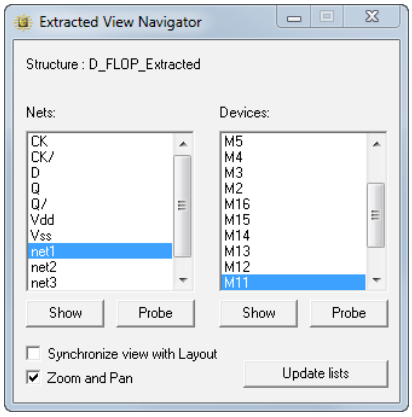
Layout Versus Schematic

LVS is a network comparator used to compare an electrical network extracted (using HLE) from a physical layout to a reference electrical network in order to detect a mis-match and therefore a physical layout error.

Locating Nets and Devices Easily

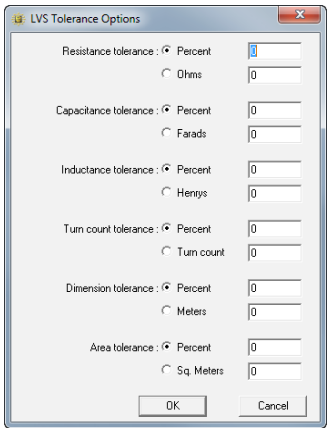
HLE also includes a navigator that allows you to easily highlight and trace networks and located devices. Combined with the LVS report, it is an easy way to locate and correct electrical problems.





Pin Swapping

By using the options or a mapping file, you can specify that certain device pins are interchangeable, for example, the two inputs of a "NAND".



Allowing Acceptable Differences

Due to certain process rules, it is sometimes impossible to re-create certain devices perfectly. Instead of modifying the original reference netlist, you can specify options and tolerance values in order to allow for acceptable differences between the two netlists.

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