DESIGN WORKSHOP TECHNOLOGIES

WHITE PAPER

New Manufacturing Techniques for Optical Components Require the Power of Traditional IC Tools with Photonic Features

Montreal, QC – January 17, 2002 – Traditional IC layout and verification tools are being used more frequently for supporting the transition from manually assembled optical components to high yield manufactured components. In addition, these tools require unique capabilities that go beyond the traditional mask layout tools capabilities.

Introduction

Over the last few years the optical component industry has embarked on a planar waveguide revolution. The basis of planar waveguide technology is to create optical waveguides on substrates utilizing manufacturing processes similar to those used in the semiconductor industry. The benefits of this technology are high yield scalable manufacturing, a platform for further optical integration and improved quality over manual assembly techniques. Planar technology is currently being used to manufacture a variety of components including AWG, VOA, OADM and SOA.

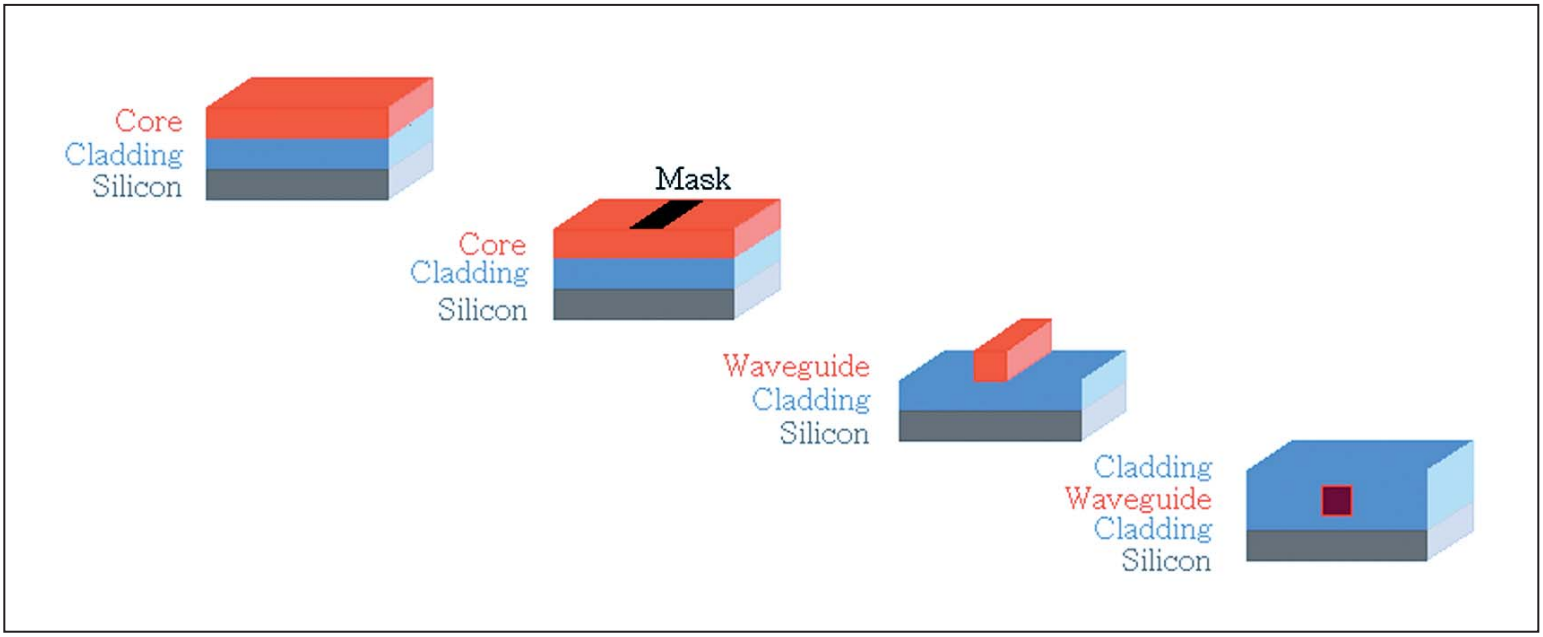

Fig. 1 – Waveguide fabrication process

Planar waveguides typically start with a lower cladding layer being deposited on the surface of a wafer of the appropriate material e.g. silicon. The core layer is then deposited on top of the lower cladding layer. The core layer has a slightly higher refractive index that keeps the light confined to the core material. A mask is then applied using standard lithographic methods to the surface of the core layer. The mask contains the pattern for the waveguide structure. The next step is to etch away the material not protected by the mask, leaving only the core waveguide pattern. A final layer of cladding with refractive index lower than the core is then added to cover the core. This technique is the same for very simple single channel waveguides to very complex multi channeled optical integrated circuits (called Planar Lightwave Circuits (PLC), Photonic Integrated Circuits (PIC), or Optical Integrated Circuits (OIC)).

There are, however, many challenges involved in creating the correct mask that will ultimately result in a circuit with the desired performance. Overcoming these challenges requires the right design methodology along with the right tools. These tools need to have proven results in laying out and verifying masks combined with specific features that address the intricacies typical of planar lightwave circuits.

Design Methodology

Computer-aided-design tools have played an important role in supporting the current design of optical components. Together the existing tools represent the Photonic Design Automation (PDA) industry. These tools have typically focused their attention on the simulation and modeling of the materials, waveguides and integrated circuits. Although the preparation of the mask is recognized as a significant step in the process, no tools have yet addressed the particular challenges involved in preparing these masks. Currently, designers are able to take their designs only so far before they are required to depend on the mask shops to interpret their designs.

Once the physical properties of the modeled waveguide have been translated to coordinates, either through the front-end modeling tool or through in-house coordinate generating functions, possibly using MatLab™ or other similar computation engines, additional layers, markings, alignments and labeling are required. The design may also require additional elements, such as pads and electrical interconnects that require a more flexible layout tool. Using the correct tool, one that is dedicated to the task can mean the difference between success and failure – and whether or not the design will reach the market in time.

Today's complex optoelectronic integrated circuits (OEIC) require increasingly more physical layers. Where a simple waveguide may only require three layers, specialized features in the design, sophisticated design processes and electrical components can contribute to components requiring ten or even twenty layers. Generating these layers is often a product of the waveguide structure or other layers. The most accurate and efficient way to generate these layers is to use powerful Boolean engines that create new layers from logical AND, OR, inverting or resizing operations. However the photonic industry has special requirements such as all angle and numerical stability that are not addressed in traditional IC design tools.

A key to reducing the time to market is to have a smooth transition between each design step. Since different tools are often best for carrying out specific design steps, an efficient way is needed for moving from one tool to another. This is especially true for creating masks, when a lot can happen that may require going back to the modeling step. For example, for complex integrated components there may be size limitations in creating the mask layout, or certain modeling parameters cannot be supported by the fabrication process, which would require changing the design specifications. The mask tool has to be aware of the manufacturing intricacies, such as grid distribution and lithographic stitching errors.

A smooth transition between design tools can most easily be achieved through a parametric approach. With this approach waveguides are specified according to their type and defined by variables and expressions. Each step of the design methodology can then refer to the same device and parameter.

Another essential component in a design methodology that reduces the time to market is a hierarchical approach to both simulation and layout. This entails creating individual cells or structures that will be instantiated through out the final design. This saves time by not having to redesign a cells, but even more critically, should a cell need to be changed, then the designer needs to make the change in only one place rather than in every location that uses that cell. Using parameterized cells can further improve productivity when a design requires multiple instances of the same cell however with slightly different parameters. In these cases a powerful scripting language can be used to automatically layout each component with its specified parameters at the correct location in the layout.

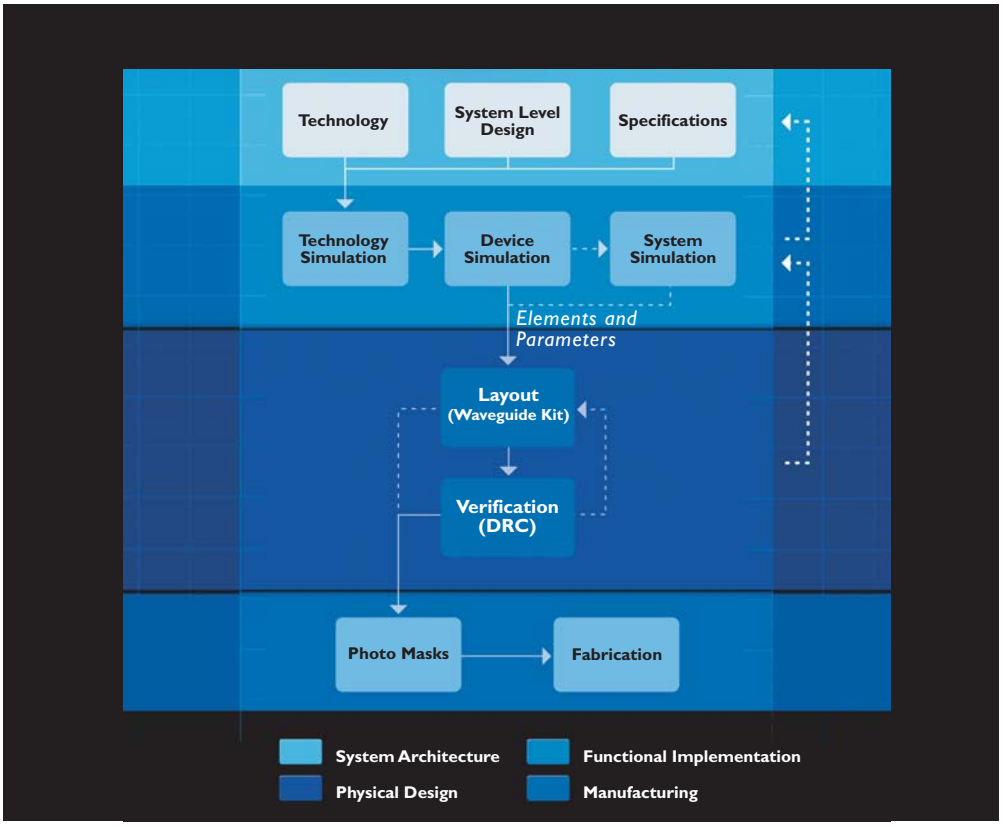

Fig. 2 – Photonic design flow

Having correctly modeled the device and created the corresponding masks is the first step in creating a new optical component. The next critical steps are fabricating the photomasks and manufacturing the components. Avoiding a lengthy process of cycling between the designer and the mask shop requires careful preparation of the GDSII file or the machine readable format (Mebes, JEOL, Cambridge) that is delivered by the designer.

For twenty years now, the last step before manufacturing an IC in the microelectronic industry has been to verify that the design rules set out by the fabrication houses have been followed. This requires a dedicated tool, the Design Rule Checker (DRC), that automatically checks these rules for the designer, it is an otherwise time consuming task that is susceptible to human errors.

Similar to the microelectronic industry the optical designer needs to be able verify that the design conforms to the manufacturers requirements. However traditional IC verification tools that were built to efficiently handle designs with only 45 and 90 degree geometries, typical of IC, are not equipped to deal with the bends and all angle geometries found in optics. Special rules, that are not found in the IC world, our also necessary. Of particular importance to designers of optical components are gaps and misalignments that can occur between the polygons that make up waveguides. Optical designers are also interested in measuring the spacing, the width or maximum bend radii of waveguides. Also, because of certain manufacturing limitations, offgrid checks are often performed. The grid defines the precision with which machines can render the waveguides. Waveguides built on a different grid will most probably be inaccurately fabricated or possibly cause unexpected light loss.

The PDA industry is at an early stage and will evolve rapidly in the next few years. As fabrication processes become more mature, verification will become more standardized and complete verification decks will be available. The integration of more components on the same wafer will also require tools to verify that the components and the links between them are layed out properly. Again similar techniques used in the EDA industry will be applied to the PDA industry to ensure that the layout matches the simulated designs with the availability of photonics specific features.

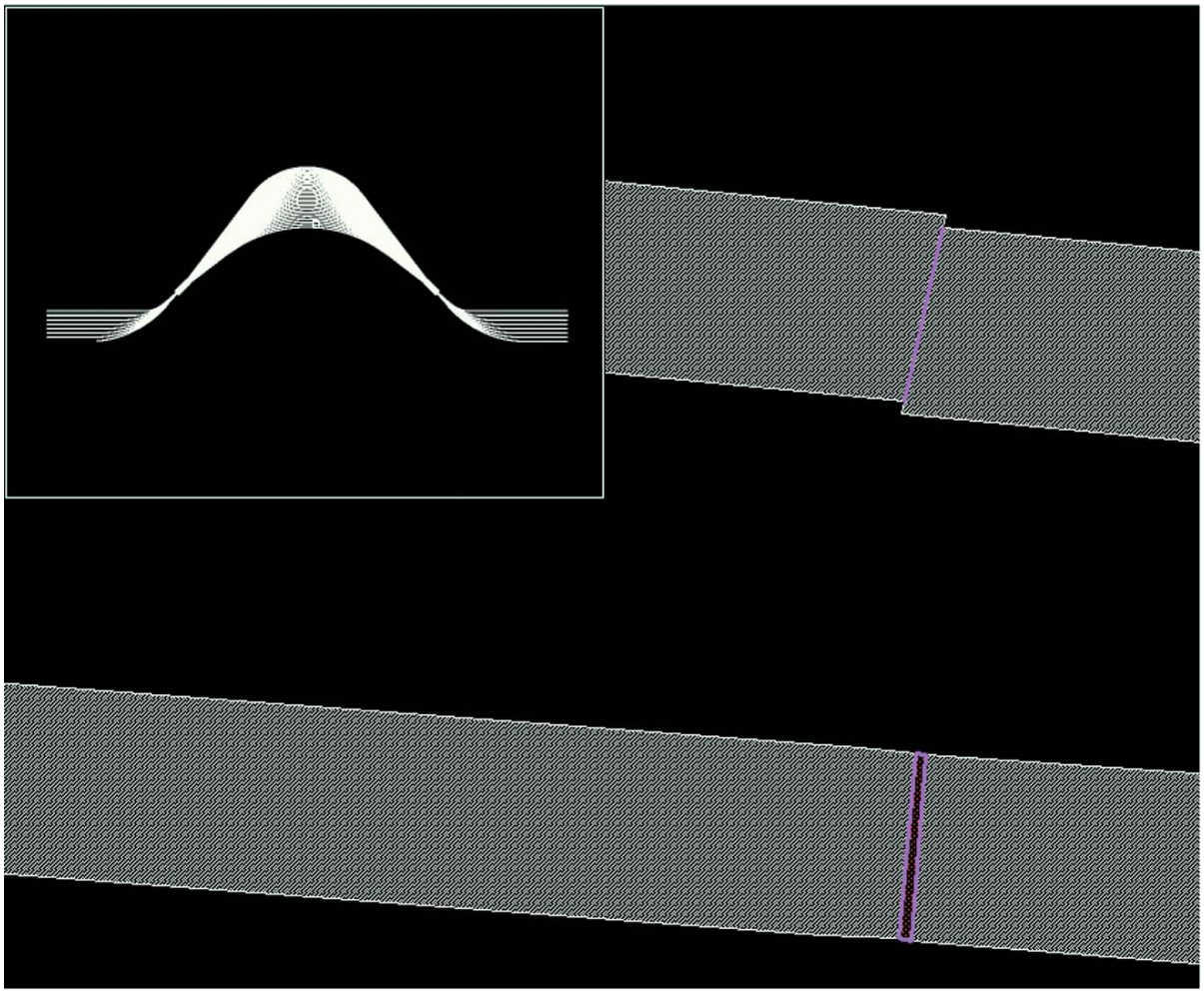

Fig. 3 – Locating errors in masks

Conclusion

Already many of the companies developing leading edge optical components have adopted design methodologies that are looking more and more like the standard methodology used in the microelectronics industry. This is not surprising since the optical component industry is going through the same transition as the printed circuit board did twenty years ago – utilizing high yield manufacturing techniques and integrating more and more devices on the same component. As this trend continues, the methodologies, libraries and verification techniques will become ever more ubiquitous. Design Workshop has already laid down the foundation for back end tools that apply to the photonic industry and will remain at the forefront of providing the tools required for the high yield manufacturing of optical components.

Contact: Design Workshop Technologies
Peter MacKenzie
514-745-0770
pmackenzie@designw.com